Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 1-6 are pending in the application, with claim 1 being the independent claims. Claims 1 and 6 are sought to be amended. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding rejections and that they be withdrawn.

Reclamation

In the Amendment and Reply Under 37 C.F.R. § 1.111 filed November 16, 2006, (hereinafter "the November 16, 2006, Reply") and the Amendment and Reply Under 37 C.F.R. § 1.116 filed February 12, 2007, (hereinafter "the February 12, 2007, Reply") Applicants amended independent claim 1 to delete, respectively, the features wherein the reset switch is configured to couple the first port directly to the second port and wherein the bistable pair of transistors is connected directly to the first supply voltage. These features had been added to independent claim 1 in the Amendment and Reply Under 37 C.F.R. § 1.116 filed June 29, 2006, (hereinafter "the June 29, 2006, Reply").

In the June 29, 2006, Reply, Applicants distinguished independent claim 1 from the teachings of U.S. Patent No. 4,521,703 to Dingwall (hereinafter "Dingwall") because Dingwall does not disclose, teach, or suggest the features wherein the reset switch is

configured to couple the first port directly to the second port and wherein the bistable pair of transistors is connected directly to the first supply voltage.

However, in addition to this distinction, Dingwall also does not disclose, teach, or suggest the feature of a bistable pair of transistors with ***both transistors*** connected directly between a reset switch and a ***first node***. Because the feature of a bistable pair of transistors with both transistors connected directly between a reset switch and a first node is sufficient to render independent claim 1 patentable over Dingwall, Applicants, in the present Amendment and Reply Under 37 C.F.R. 1.111, amended independent claim 1 to add "with both transistors" to the feature of "a bistable pair of transistors connected directly between a reset switch and a first node" to recite the feature of "a bistable pair of transistors with both transistors connected directly between a reset switch and a first node[.]" (The feature wherein the reset switch is configured to couple the first port directly to the second port had been deleted in the November 16, 2006, Reply and the feature wherein the bistable pair of transistors is connected directly to the first supply voltage had been deleted in the February 12, 2007, Reply.)

Applicants affirmatively rescind the distinction from the teachings of Dingwall based upon the features wherein the reset switch is configured to couple the first port directly to the second port and wherein the bistable pair of transistors is connected directly to the first supply voltage.

Rejections Under 35 U.S.C. § 102

The Office Action rejected claims 1, 2, and 4-6 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,977,798 to Zerbe (hereinafter "Zerbe"). (*See* Office Action at p. 2.) Applicants respectfully traverse these rejections.

Amended independent claim 1 recites (emphasis added):

> A latch circuit, comprising:
>
> *a bistable pair of transistors with both transistors connected directly between a reset switch and a* ***first node***, and having a first port for receiving a first current signal and producing a first output voltage, and a second port for receiving a second current signal and producing a second output voltage; and
>
> a vertical latch having a first transistor connected directly to a second transistor, said *second transistor connected directly to said* ***first node***, said first transistor connected directly to a second node, said first transistor connected to said first port so that, when said first transistor is turned on, a current flows through said first transistor and said first port, wherein said first transistor is a first type, said second transistor is a second type, and said first type is different from said second type.

Zerbe does not disclose, teach, or suggest a latch circuit having a bistable pair of transistors and a vertical latch in which the bistable pair of transistors has both transistors connected directly between a reset switch and a first node and the vertical latch has a first transistor connected directly to a second transistor with the second transistor connected directly to the first node, the first transistor connected directly to a second node, and the first transistor connected to the first port so that, when the first transistor is turned on, a current flows through the first transistor and the first port, and such that the first transistor is a first type, the second transistor is a second type, and the first type is different from the second type.

Therefore, Zerbe does not anticipate claim 1. Because claims 2 and 4-6 depend upon claim 1 and because of the additional distinctive features of claims 2 and 4-6, these claims are

also not anticipated by Zerbe. Accordingly, Applicants respectfully request that the Examiner reconsider and remove the rejections of claims 1, 2, and 4-6 under 35 U.S.C. § 102(b) and pass these claims to allowance.

Rejections Under 35 U.S.C. § 103

The Office Action rejected claim 3 under 35 U.S.C. § 103(a) as being unpatentable over Zerbe in view of U.S. Patent Application Publication No. 2001/0048141 to Lin *et al.* (hereinafter "Lin"). (*See* Office Action at p. 3.) Applicants respectfully traverse this rejection.

Claim 3 depends upon claim 1. As stated above, Zerbe does not disclose, teach, or suggest a latch circuit having a bistable pair of transistors and a vertical latch in which the bistable pair of transistors has both transistors connected directly between a reset switch and a first node and the vertical latch has a first transistor connected directly to a second transistor with the second transistor connected directly to the first node, the first transistor connected directly to a second node, and the first transistor connected to the first port so that, when the first transistor is turned on, a current flows through the first transistor and the first port, and such that the first transistor is a first type, the second transistor is a second type, and the first type is different from the second type. Lin does not overcome this deficiency.

Therefore, claim 1 is patentable over Zerbe in view of Lin. Because claim 3 depends upon claim 1 and because of the additional distinctive features of claim 3, this claim is also patentable over Zerbe in view of Lin. Accordingly, Applicants respectfully request that the

Examiner reconsider and remove the rejection of claim 3 under 35 U.S.C. § 103(a) and pass this claim to allowance.

Conclusion

All of the stated grounds of rejection have been properly traversed. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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